Characterization and Integration of Porous Extra Low-k (XLK) Dielectrics

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Abstract

Porous XLK dielectric films have been characterized and integrated into one level metal Cu damascene test structures. The material shows reduced dielectric constant as well as lower modulus compared with dense HSQ. Initial one level metal Cu/XLK damascene integration studies demonstrate the feasibility and issues associated with the use of porous low-k materials. Parametric test data show good capacitance and leakage current distributions.

Introduction

As device scaling continues into the deep-sub-micron region, the gain in device speed at the gate level is offset by propagation delays at metal interconnects due to the increased RC time constant. The RC time delay can be reduced by the incorporation of low dielectric constant (k) materials and/or high conductivity metals. The use of low-k dielectric materials also lowers power consumption and reduces crosstalk (1).

There are numerous low-k dielectric candidates available with dielectric constant in the range between 2.4 and 4.0 (2). As predicted by the International Technology Roadmap for Semiconductors (3), continued scaling of devices will require extra-low-k materials with dielectric constant as low as 1.5. One of the ways to obtain lower dielectric constant is fluorination of either inorganic or organic dielectric materials. However, the lowest dielectric constant available for fluorinated dense materials is around k ~1.9 (Teflon®) and none of the current approaches using dense materials is expected to achieve k values lower than that. Incorporation of pores into dense materials to make them porous is another attractive method to obtain extra-low-k materials (4). For a porous material, the dielectric constant is a combination of air and that of the dense phase, and it has the potential to drive the dielectric constant significantly below 2. To meet performance goals, future technology nodes will require materials with progressively lower dielectric constant. A change in dielectric material for each technology node increases process and equipment complexity and development cost. It is desirable to have one kind of material that can meet the requirements for multiple future technology nodes. Porous dielectric materials offer the extendibility to multiple technology nodes because they have tunable dielectric constant.

The Dow Corning® XLK material is a porous dielectric and has been evaluated for advanced interconnect applications.

Thin Film Deposition

All data presented in this paper were obtained on XLK films deposited at Dow Corning. The films were deposited via a spin on process. The chemical formulation contains HSQ resin, a high boiling point solvent, and a low boiling point solvent. The film formation principles are 1) Gellation in the presence of high boiling point solvent at ambient conditions; 2) Removing solvent without collapsing resin structure; 3) Building strong network structure during final cure. The film was first spin coated onto a wafer with 2000 RPM – 4000 RPM spin speed under typical spin coating conditions. The wafer then went into a wet ammonia treatment chamber for 30 – 120 seconds depending on the chamber conditions. In the wet ammonia treatment chamber, which is at room temperature, the following gellation reaction occurs,

$$SiH + H_2O \rightarrow SiOH + SiOH \rightarrow SiOSi\ (Gel)\ and\ /\ or$$
$$SiH + SiOH \rightarrow SiOSi\ (Gel)$$

The optimum treatment time depends on a number of factors which include, polarity of solvents, chamber size, chamber treatment conditions, and ammonia and water concentration. After the wet ammonia treatment, the film was cured at 450 °C for 1 hour in a low oxygen (< 10 ppm) atmosphere.

Materials Property Characterization

Material properties of Dow Corning® XLK films are summarized in Table 1. Dielectric constant of the material was measured using MIM structures formed by depositing Al dots directly on a XLK film through a shadow mask. The XLK film was on a heavily doped Si substrate. Film thickness was determined by cross-sectional SEM under each Al dot. Care has been taken as to minimize film shrinkage caused by the SEM electron beam. Adhesion of XLK films to various substrates was evaluated using tape pull and modified edge lift-off tests (m-ELT) (5). Specular X-ray reflectance (SXR) and small angle neutron scattering (SANS) techniques (6,7) were used to measure coefficient of thermal expansion (CTE), porosity, density, average pore size, and pore connectivity. Thermal conductivity of the film was determined by a 3ω method (8). The Young's modulus of XLK films measured by nano-indentation is smaller than that of dense HSQ.

Table 1. Material Properties of XLK Film (1 micron in thickness)

Material Property	Dow Corning® XLK
Dielectric Constant	2.19 ± 0.10
Adhesion	
Tape Test	SiO_2: Pass; Ta: Pass; Si_3N_4: Pass; TaN: Pass
m-ELT K_{IC} (MPa-$m^{1/2}$)	SiO_2: 0.221±0.015; Ta: 0.203 ± 0.014 SiN: 0.252±0.026; TaN: 0.220± 0.013
Young's Modulus (GPa)	2.5 (nano-indentation)
CTE (ppm/°C by SXR)	<4 (vertical)
Stress @ 25 °C (MPa)	21
Porosity (% by SANS)	59.5%
Average Pore Size (nm by SANS)	2.4
Pore Connectivity (SANS)	100%
Density (g/cc)	0.88
Thermal Conductivity (W/mK)	0.22

Blanket film CMP was used to test the film adhesion and mechanical strength. A 500 nm XLK film was deposited on a 100 nm Si_3N_4 / 550 nm thermal SiO_2 / Si substrate. The XLK film was capped with a 100 nm CVD SiO_2 film followed by the deposition of a 25 nm TaN barrier layer and a 100 nm PVD Cu seed. Delamination occurred before the complete removal of Cu even under mild (1-2 PSI) CMP conditions. XSEM inspection of the delaminated areas indicates the

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SiO_2 cap layer has been removed due to poor adhesion to the XLK film, surface contamination, or cohesive failure of the XLK film. However, the next section of this paper will show a patterned XLK 1LM structure without delamination or defects even in the field region after CMP.

In a separate thermal stability test, a double layer XLK film stack with CVD SiO_2 caps on top of each XLK layer was annealed at 400 °C for 1 hour, and no defects were observed.

Integration

One level metal Cu damascene integration studies have been conducted with the XLK film. The starting substrate was a 100 nm CVD Si_3N_4 on top of 550 nm thermal SiO_2 on a Si wafer. 700 nm of XLK film was deposited followed by another 100 nm of CVD SiO_2 cap layer. The cap layer deposition process was optimized to improve adhesion to the XLK film while minimizing damages due to the oxidizing plasma. FTIR was used to monitor plasma damages to the XLK film. The wafers were patterned using a DUV process. A two step etch recipe was used to etch trenches in the dielectric film stack; the first step was to open the cap oxide layer, and the second step was used to etch the XLK film and stop at the Si_3N_4 under layer. An XSEM image of 0.35 µm / 0.40 µm (line/space) XLK trenches after etch is shown in Fig. 1, which displays reasonably good sidewall etch profiles. Photo-resist ash was done by using a low power, low temperature, and low pressure HDP process. FTIR spectra were taken on bare XLK film, after cap oxide deposition, and post etch/ash. The integrated SiHx peak areas after each process are listed in Table 2. The post etch/ash spectrum was taken on a patterned wafer. The post etch/ash SiHx integrated area was calculated by normalizing the SiOSi peak areas to that in the post oxide cap spectrum. The SiHx peak shows slight reduction after oxide cap deposition. The post etch/ash FTIR spectrum displays a much smaller Si-H peak intensity and appearance of a small peak due to moisture adsorption. Clearly an O_2 free ash process is needed to minimize the damage to XLK films.

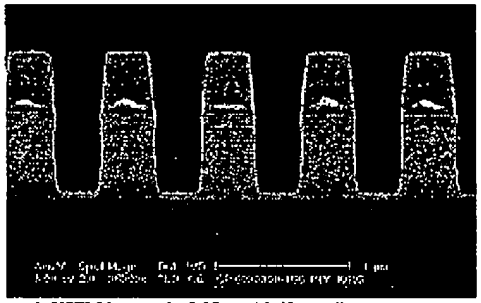

Figure 1. XSEM image of a 0.35 µm / 0.40 µm (line/space) etched XLK trench.

Table 2. Integrated SiHx peak areas of bare XLK film, after cap oxide deposition, and post etch/ash.

Process	Normalized SiHx Area
Blanket XLK	2.099
Post SiO_2 Cap	1.938
Post Etch / Ash	1.338

A 25 nm TaN barrier layer and a 100 nm Cu seed were deposited at 50 °C on all wafers. The wafers were baked for 120 seconds at 350 °C prior to the PVD barrier and Cu deposition. One micron of electroplated Cu was deposited afterwards.

CMP is one of the most challenging process steps for porous materials because of the downward and shear stresses applied onto wafers and the relatively low mechanical strength of porous materials. As mentioned in the previous section, the XLK film did not pass the blanket film CMP tests. However, unlike in the blanket film CMP tests, no visual defects were observed on patterned wafers during and after the CMP process. Fig. 2 shows an optical microscope image of a field region on one of the wafers after polish. Neither delamination nor other defects are observed.

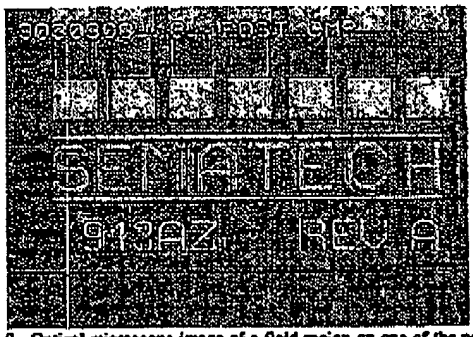

Figure 2. Optical microscope image of a field region on one of the patterned XLK wafers after polish. Neither delamination nor other defects are observed.

Electrical tests were performed after CMP. Then, a 100 nm CVD Si_3N_4 layer was deposited to passivate the structures. The wafers were baked for 120 seconds at 400 °C before the Si_3N_4 deposition. Fig. 3 shows XSEM images of 0.35 µm / 0.40 µm (line/space) trenches of a completed XLK 1LM structure. Probe bond pads were patterned and etched. The wafers were then electrically tested. After annealing for 1 hour at 400 °C under N_2 atmosphere in an oven (thermal cycle 1), electrical tests were once again performed on the wafers. The wafers were further annealed for 1 hour at 400 °C under N_2 atmosphere for 3 cycles in the same oven (thermal cycle 2) and electrically tested for the last time.

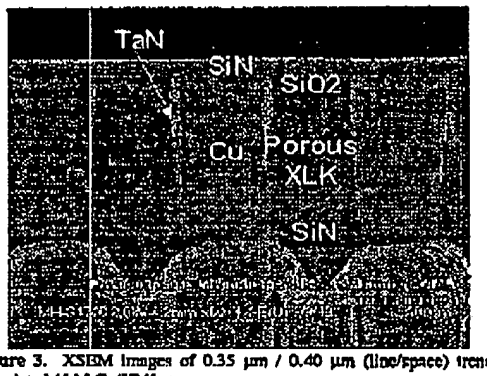

Figure 3. XSEM images of 0.35 µm / 0.40 µm (line/space) trenches in a completed 1LM Cu/XLK structure.

Parameteric Test Results

Figure 4 shows the line to line capacitance distribution measured on 0.35 µm / 0.4 µm (line/space) and 100 µm long COMB structures. Each COMB has 84 fingers. After Si_3N_4 passivation, the capacitance first increased from the post CMP values. It is primarily due to the fact that Si_3N_4 replaces air immediately above the dielectric between Cu lines and Si_3N_4 has much higher dielectric constant than that of air. The fringing field increases the whole capacitance distribution. After the first thermal annealing cycle at 400 °C, the capacitance shows significant decrease and drops even below the post CMP values. The second thermal cycle brings further reduction in capacitance. This shows that the XLK films probably had some amount of moisture adsorbed. Annealing outgasses the moisture and reduces the capacitance. The moisture absorption noticed here is perhaps caused by the material itself and damages introduced by the processes such as etch/ash etc..

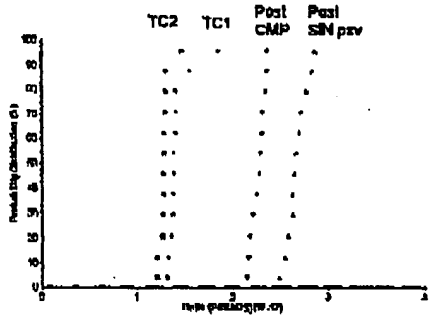

Figure 4. Line to line capacitance distribution measured on 0.35 µm / 0.4 µm (line/space) and 100 µm long COMB structures. Each COMB has 84 fingers. (TC1 = post thermal cycle 1; TC2 = post thermal cycle 2).

The line to line leakage current distribution was measured at 5 V on the same COMB structures as used for capacitance measurements. The results are displayed in Fig. 5. The leakage current decreases from post CMP to post SiN passivation, post thermal cycle one, and post thermal cycle two. Each subsequent step after CMP involved heating the wafer at higher temperatures. The decrease in leakage current can be simply explained by moisture outgassing during these process steps. The Si_3N_4 also plays certain role in decreasing the leakage current by passivating the dielectric between Cu lines.

Figure 6 shows cross sectional TEM and EDX analysis results of 0.35 µm / 0.4 µm (line/space) trenches on finished XLK 1LM structures after thermal annealing. No Cu diffusion into the XLK dielectric was detected, indicating good barrier integrity.

Conclusions

Porous materials are needed to further extend interconnect dielectrics into the extra-low-k region. Optimization of the CMP, etch, ash, clean, and other processes are necessary to avoid mechanical and chemical damages to porous low-k materials. SEMATECH evaluation results showed the feasibility of integrating the XLK porous material into Cu damascene test structures.

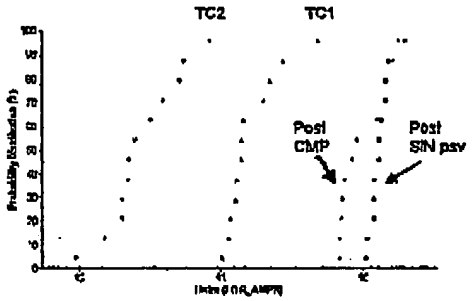

Figure 5. Line to line leakage current distribution measured at 5 V on 0.35 µm / 0.4 µm (line/space) and 100 micron long COMB structures. Each COMB has 84 fingers. (TC1 = post thermal cycle 1; TC2 = post thermal cycle 2)

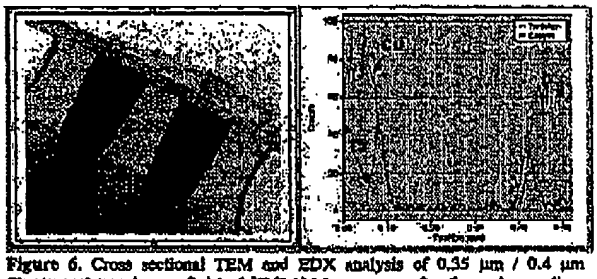

Figure 6. Cross sectional TEM and EDX analysis of 0.35 µm / 0.4 µm (line/space) trenches on finished XLK 1LM structures after thermal annealing. No Cu diffusion into the XLK dielectric was detected.

Acknowledgments

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